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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,122	03/24/2004	Yue-Der Chih	N1280-00130(TSMC2003-979)	4506

7590 04/27/2005  
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EXAMINER

TON, MY TRANG

ART UNIT PAPER NUMBER

2816

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/808,122

Applicant(s)

CHIH ET AL.

Examiner

My-Trang N. Ton

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 12-17 is/are allowed.
- 6) ☒ Claim(s) 1-6, 8-11 and 18-21 is/are rejected.
- 7) ☒ Claim(s) 7 and 22 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

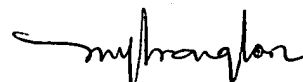
### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 March 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

  
MY-TRANG NUTON  
PRIMARY EXAMINER

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 04/12/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

## **DETAILED ACTION**

### ***Drawings***

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Objections***

Claim 19 is objected to because of the following informalities: last line, after "transistors", -- ; -- should be replaced with -- . --.

### ***Claim Rejections - 35 USC § 112***

Claims 3-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 3, the limitation "the transistors are N type, and the control voltage is coupled to the gate of transistor that is directly coupled to the high operating voltage" is misdescriptive of the present invention since such limitation is not seen as recited therein. In order to avoid any confusion, Applicant is required to particularly point out how this limitation reads on the circuit arrangement of the drawings.

Claim 5 is similarly rejected as claim 3: the limitation "the transistors are P type, and the control voltage is coupled to the gate of transistor that is directly coupled to the low voltage" is misdescriptive of the present invention since such limitation is not seen as recited therein. In order to avoid any confusion, Applicant is required to particularly point out how this limitation reads on the circuit arrangement of the drawings.

Claims 4 and 6 are rendered indefinite by the deficiencies of claims 3 and 5.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 8, 10, 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Lall et al (U.S Patent No. 6,370,071) cited in PTOL 1449.

Lall et al discloses in Fig. 4 a high voltage CMOS switch circuit including:

Regarding claim 1: one (P2) or more transistors (P2, P4) of a same type connected in series and being operable with a normal operating voltage (EN) and a high operating voltage (Vpp);

a high operating voltage (Vpp) coupled to a first end of the device (first end coupled to P2) of the device structure (300);

a low voltage (Ground) coupled to a second end (coupled to N2); and

one (hvb) or more control voltages controllably coupled to the gates of the transistors (hvb coupled to gate of P2);

wherein at least one of the control voltages (hvb) coupled to the gate of at least one transistor (P2) is raised to a medium voltage level ( $V_{pp} - \text{threshold P1,P3}$ ) that is higher than a normal operating voltage ( $V_{EN}$ ) when operating under the high operating voltage ( $V_{pp}$ ) for tolerating stress imposed thereon by the high operating voltage (when N1 is OFF,  $hvb = V_{pp} - \text{threshold P1,P3}$  that is higher than  $V_{EN}$  when operating under  $V_{pp}$ ).

Regarding claim 2: the medium voltage level is about one half of the high operating voltage ( $hvb = V_{pp} - \text{threshold of P1,P3}$  is about one half of the high operating voltage  $V_{pp}$  (when  $V_{pp} = 3.3V$ )).

Regarding claim 8: the high operating voltage is above 10V ( $V_{pp}$  is pumped up to 13 volts, see col. 5, line 2-5).

Regarding claim 10: the stress is a gated stress (P2, P4).

Regarding claim 18:

a first cascade device structure (P2, P4) having one (P2) or more (P2, P4) P type transistors connected in series with one end thereof connected to the high operating voltage (P2 connected to  $V_{pp}$ ); and

one (hvb) or more control voltages controllably coupled to the gates of the transistors (hvb coupled to gate of P2) in the first cascade device structure (P2) for raising voltages on one (P2) or more gates of the transistors to one or more medium values ( $hvb = V_{pp} - \text{threshold P1,P3}$ ) that are above the normal operating voltage ( $V_{EN}$ ) for tolerating voltage stress imposed by the high operating voltage (when N1 is OFF,  $hvb = V_{pp} - \text{threshold P1, P3}$  that is higher than  $V_{EN}$  when operating under  $V_{pp}$ );

wherein the P type transistors have separated N wells (see col. 2, lines 52-54, and col. 5, line 66 – col. 6, line 3).

Regarding claim 19: a second cascade device structure (N4, N2) in series with the first cascade device structure (P2, P4) at its other end having one or more N type transistors (N4, N2).

Regarding claim 20: the control voltages (hvb, Vcc, ENB) for the first and second cascade device structure (P2, P4, N4, N2) are controlled separately depending on the input signal (EN).

Regarding claim 21: the second cascade device structure (N4, N2) is further connected to a grounding voltage (Ground).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lall et al as applied to claims 1 and 8 above.

As stated above, every element of the claimed invention recited in above claims can be seen in the circuit of Lall. However, this reference does not specially show “the normal operating voltage is below 2V” as recited in claim 9 and “the stress is a gated stress” as recited in claim 11.

Although Lall et al do not expressly state the value for the normal operating voltage, this difference is not of patentable merit because it is notoriously well known in the art that different values for the operating voltage can be selected in order to produce correspondingly different output values. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the normal operating voltage EN is below 2 volts in realizing the circuit of the Lall et al reference for the purpose of producing different output values when different values of the operating voltage is selected.

Regarding the limitation "the stress is a drain stress" recited in claim 11: this appears to be obvious variations (i.e., not patentably distinct) to limitations "the stress is a gated stress". Therefore, it would have been obvious to one of ordinary skill in the art to employ (the stress is a drain stress for P2, P4), as they appear to be obvious variations (not patentably distinct) and yielding same functional device.

#### ***Allowable Subject Matter***

Claims 7 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims namely: "the control voltages are determined so that the stress imposed by the high voltage is about equally divided by the transistors in the device structure" (claim 7); "an input module ... raised to a predetermined medium value" (claim 22).

Claims 12–17 are allowable over the prior art of record. None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims namely: “one or more control voltages controllably coupled to the gates of the transistors in the first and second cascade device ... for tolerating voltage stress imposed by the high operating voltage” in combination with “a first cascade device structure” and “a second cascade device structure” as recited in claim 12.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



My-Trang N. Ton  
Primary Examiner  
Art Unit 2816

April 21, 2005